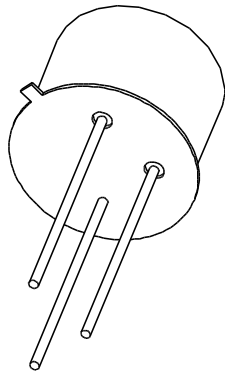


# DATA SHEET



## **BFY50; BFY51; BFY52** NPN medium power transistors

Product specification  
Supersedes data of September 1994  
File under Discrete Semiconductors, SC04

1997 Apr 22

# NPN medium power transistors

# BFY50; BFY51; BFY52

### FEATURES

- High current (max. 1 A)
- Low voltage (max. 35 V).

### APPLICATIONS

- General purpose industrial applications.

### DESCRIPTION

NPN medium power transistor in a TO-39 metal package.

### PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

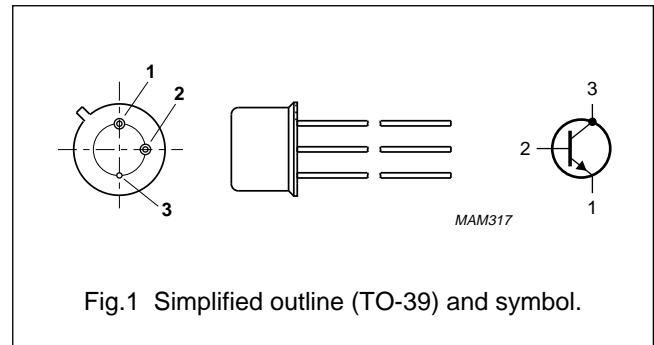


Fig.1 Simplified outline (TO-39) and symbol.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
V <sub>CBO</sub>	collector-base voltage	open emitter					
	BFY50		–	–	80	V	
	BFY51		–	–	60	V	
V <sub>CEO</sub>	collector-emitter voltage	open base					
	BFY50		–	–	35	V	
	BFY51		–	–	30	V	
	BFY52		–	–	20	V	
I <sub>CM</sub>	peak collector current		–	–	1	A	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	–	–	800	mW	
		T <sub>case</sub> ≤ 100 °C	–	–	2.86	W	
h <sub>FE</sub>	DC current gain	I <sub>C</sub> = 150 mA; V <sub>CE</sub> = 10 V					
	BFY50		30	112	–		
	BFY51		40	123	–		
f <sub>T</sub>	transition frequency	I <sub>C</sub> = 50 mA; V <sub>CE</sub> = 10 V; f = 100 MHz					
			BFY50	60	–	–	MHz
			BFY51; BFY52	50	–	–	MHz

## NPN medium power transistors

## BFY50; BFY51; BFY52

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter			
	BFY50		–	80	V
	BFY51		–	60	V
	BFY52		–	40	V
V <sub>CEO</sub>	collector-emitter voltage	open base			
	BFY50		–	35	V
	BFY51		–	30	V
	BFY52		–	20	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	6	V
I <sub>C</sub>	collector current (DC)		–	1	A
I <sub>CM</sub>	peak collector current		–	1	A
I <sub>BM</sub>	peak base current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	–	800	mW
		T <sub>case</sub> ≤ 25 °C	–	5	W
		25 °C < T <sub>case</sub> < 100 °C	–	2.86	W
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	200	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	in free air	220	K/W
R <sub>th j-c</sub>	thermal resistance from junction to case		35	K/W

## NPN medium power transistors

## BFY50; BFY51; BFY52

**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector cut-off current BFY50	$I_E = 0; V_{CB} = 60\text{ V}$	–	–	50	nA
		$I_E = 0; V_{CB} = 60\text{ V}; T_j = 100\text{ }^\circ\text{C}$	–	–	2.5	$\mu\text{A}$
		$I_E = 0; V_{CB} = 80\text{ V}$	–	–	500	nA
		$I_E = 0; V_{CB} = 80\text{ V}; T_j = 100\text{ }^\circ\text{C}$	–	–	30	$\mu\text{A}$
$I_{CBO}$	collector cut-off current BFY51	$I_E = 0; V_{CB} = 40\text{ V}$	–	–	50	nA
		$I_E = 0; V_{CB} = 40\text{ V}; T_j = 100\text{ }^\circ\text{C}$	–	–	2.5	$\mu\text{A}$
		$I_E = 0; V_{CB} = 60\text{ V}$	–	–	500	nA
		$I_E = 0; V_{CB} = 60\text{ V}; T_j = 100\text{ }^\circ\text{C}$	–	–	30	$\mu\text{A}$
$I_{CBO}$	collector cut-off current BFY52	$I_E = 0; V_{CB} = 30\text{ V}$	–	–	50	nA
		$I_E = 0; V_{CB} = 30\text{ V}; T_j = 100\text{ }^\circ\text{C}$	–	–	2.5	$\mu\text{A}$
		$I_E = 0; V_{CB} = 40\text{ V}$	–	–	500	nA
		$I_E = 0; V_{CB} = 40\text{ V}; T_j = 100\text{ }^\circ\text{C}$	–	–	30	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	50	nA
		$I_C = 0; V_{EB} = 5\text{ V}; T_j = 100\text{ }^\circ\text{C}$	–	–	2.5	$\mu\text{A}$
		$I_C = 0; V_{EB} = 6\text{ V}$	–	–	500	nA
$h_{FE}$	DC current gain BFY50	$I_C = 10\text{ mA}; V_{CE} = 10\text{ V}$	20	–	–	
		$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 500\text{ mA}; V_{CE} = 10\text{ V}$	20	–	–	
		$I_C = 1\text{ A}; V_{CE} = 10\text{ V}$	15	–	–	
$h_{FE}$	DC current gain BFY51	$I_C = 10\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$	40	–	–	
		$I_C = 500\text{ mA}; V_{CE} = 10\text{ V}$	25	–	–	
		$I_C = 1\text{ A}; V_{CE} = 10\text{ V}$	15	–	–	
$h_{FE}$	DC current gain BFY52	$I_C = 10\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$	60	–	–	
		$I_C = 500\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 1\text{ A}; V_{CE} = 10\text{ V}$	15	–	–	

## NPN medium power transistors

## BFY50; BFY51; BFY52

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CEsat}$	collector-emitter saturation voltage BFY50	$I_C = 10 \text{ mA}; I_B = 1 \text{ mA}$	–	–	200	mV
		$I_C = 150 \text{ mA}; I_B = 15 \text{ mA}$	–	–	200	mV
		$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}$	–	–	700	mV
		$I_C = 1 \text{ A}; I_B = 100 \text{ mA}$	–	–	1	V
$V_{CEsat}$	collector-emitter saturation voltage BFY51; BFY52	$I_C = 10 \text{ mA}; I_B = 1 \text{ mA}$	–	–	200	mV
		$I_C = 150 \text{ mA}; I_B = 15 \text{ mA}$	–	–	350	mV
		$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}$	–	–	1	V
		$I_C = 1 \text{ A}; I_B = 100 \text{ mA}$	–	–	1.6	V
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 1 \text{ mA}$	–	–	1.2	V
		$I_C = 150 \text{ mA}; I_B = 15 \text{ mA}$	–	–	1.3	V
		$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}$	–	–	1.5	V
		$I_C = 1 \text{ A}; I_B = 100 \text{ mA}$	–	–	2	V
$C_c$	collector capacitance	$I_E = I_e = 0; V_{CB} = 10 \text{ V}; f = 1 \text{ MHz}$	–	7	12	pF
$f_T$	transition frequency BFY50 BFY51; BFY52	$I_C = 50 \text{ mA}; V_{CE} = 10 \text{ V};$ $f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$	60	140	–	MHz
			50	–	–	MHz
<b>Switching times (between 10% and 90% levels)</b>						
$t_{on}$	turn-on time	$I_{Con} = 150 \text{ mA}; I_{Bon} = 15 \text{ mA};$ $I_{Boff} = -15 \text{ mA}$	–	55	–	ns
$t_d$	delay time		–	15	–	ns
$t_r$	rise time		–	40	–	ns
$t_{off}$	turn-off time		–	360	–	ns
$t_s$	storage time		–	300	–	ns
$t_f$	fall time		–	60	–	ns

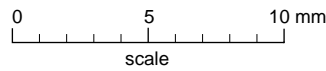
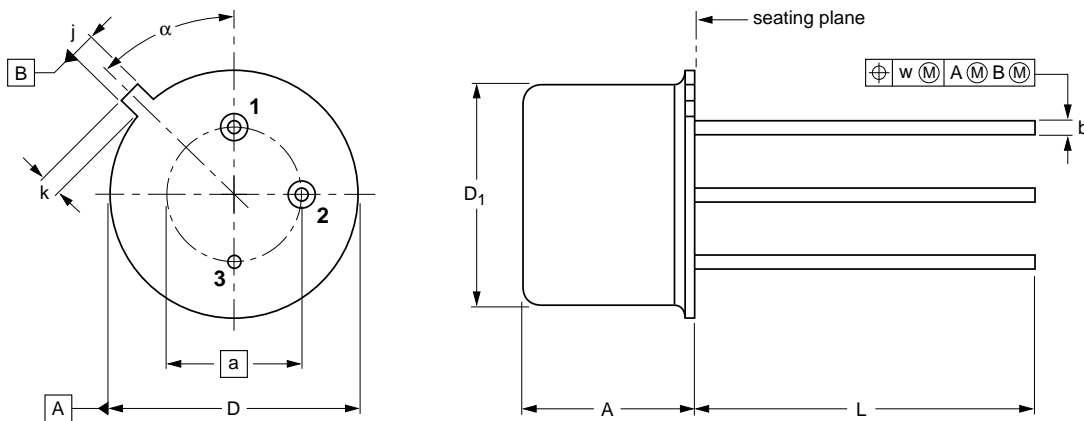
NPN medium power transistors

BFY50; BFY51; BFY52

PACKAGE OUTLINE

Metal-can cylindrical single-ended package; 3 leads

SOT5/11



DIMENSIONS (mm are the original dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	α
mm	6.60 6.35	5.08	0.48 0.41	9.39 9.08	8.33 8.18	0.85 0.75	0.95 0.75	14.2 12.7	0.2	45°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT5/11		TO-39				97-04-11

## NPN medium power transistors

BFY50; BFY51; BFY52

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
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