National Semiconductor

# DM54/74S573
# (1024 x 4) 4096-Bit TTL PROM

## General Description

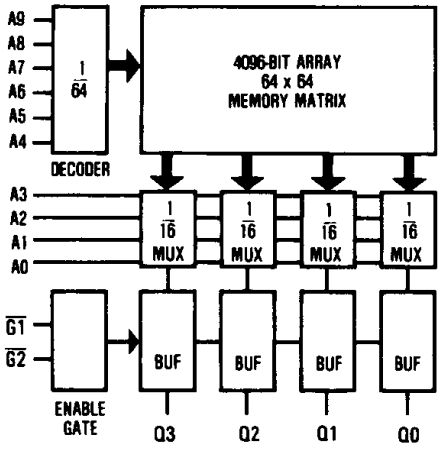
This Schottky memory is organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

## Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® Outputs

## Block Diagram

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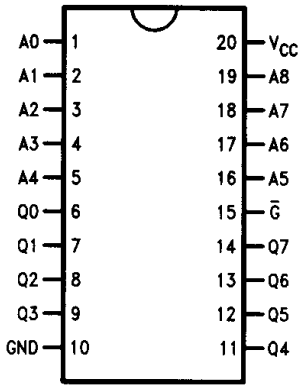
**Pin Names**

| | |
|---|---|
| A0–A9 | Addresses |
| $\overline{G1}$–$\overline{G2}$ | Output Enables |
| GND | Ground |
| Q0–Q3 | Outputs |
| $V_{CC}$ | Power Supply |

## Connection Diagrams

**Dual-In-Line Package**

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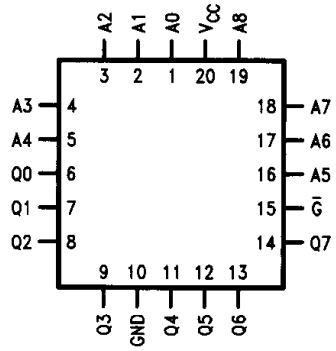
**Top View**

**Order Number**
**DM54/74S573J, 573AJ, 573BJ**
**DM74S573N, 573AN, 573BN**
**See NS Package Number J18A or N18A**

**Plastic Leaded Chip Carrier (PLCC)**

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**Top View**

**Order Number**
**DM74S573V, 573AV, 573BV**
**See NS Package Number V20A**

## Ordering Information

**Commercial Temp Range (0°C to +70°C)**

| Parameter/Order Number | Max Access Time (ns) |
|---|---|
| DM74S573AJ | 45 |
| DM74S573BJ | 35 |
| DM74S573J | 60 |
| DM74S573AN | 45 |
| DM74S573BN | 35 |
| DM74S573N | 60 |
| DM74S573AV | 45 |
| DM74S573BV | 35 |
| DM74S573V | 60 |

**Military Temp Range (−55°C to +125°C)**

| Parameter/Order Number | Max Access Time (ns) |
|---|---|
| DM54S573AJ | 60 |
| DM54S573BJ | 50 |
| DM54S573J | 75 |

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage (Note 2) | −0.5V to +7.0V |
| Input Voltage (Note 2) | −1.2V to +5.5V |
| Output Voltage (Note 2) | −0.5V to +5.5V |
| Storage Temperature | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 300°C |

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

**Note 2:** These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

## Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | | |
| Military | 4.50 | 5.50 | V |
| Commercial | 4.75 | 5.25 | V |
| Ambient Temperature ($T_A$) | | | |
| Military | −55 | +125 | °C |
| Commercial | 0 | +70 | °C |
| Logical "0" Input Voltage | 0 | 0.8 | V |
| Logical "1" Input Voltage | 2.0 | 5.5 | V |

## DC Electrical Characteristics (Note 1)

| Symbol | Parameter | Conditions | DM54S573 | | | DM74S573 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $I_{IL}$ | Input Load Current | $V_{CC}$ = Max, $V_{IN}$ = 0.45V | | −80 | −250 | | −80 | −250 | μA |
| $I_{IH}$ | Input Leakage Current | $V_{CC}$ = Max, $V_{IN}$ = 2.7V | | | 25 | | | 25 | μA |
| | | $V_{CC}$ = Max, $V_{IN}$ = 5.5V | | | 1.0 | | | 1.0 | mA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | | 0.35 | 0.50 | | 0.35 | 0.45 | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.80 | | | 0.80 | V |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | | 2.0 | | | V |
| $V_C$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_{IN}$ = −18 mA | | −0.8 | −1.2 | | −0.8 | −1.2 | V |
| $C_I$ | Input Capacitance | $V_{CC}$ = 5.0V, $V_{IN}$ = 2.0V<br>$T_A$ = 25°C, 1 MHz | | 4.0 | | | 4.0 | | pF |
| $C_O$ | Output Capacitance | $V_{CC}$ = 5.0V, $V_O$ = 2.0V<br>$T_A$ = 25°C, 1 MHz, Outputs Off | | 6.0 | | | 6.0 | | pF |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max, Input Grounded<br>All Outputs Open | | 100 | 140 | | 100 | 140 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_O$ = 0V, $V_{CC}$ = Max<br>(Note 2) | −20 | | −70 | −20 | | −70 | mA |
| $I_{OZ}$ | Output Leakage (TRI-STATE) | $V_{CC}$ = Max, $V_O$ = 0.45V to 2.4V<br>Chip Disabled | | | +50 | | | +50 | μA |
| | | | | | −50 | | | −50 | μA |
| $V_{OH}$ | Output Voltage High | $I_{OH}$ = −2.0 mA | 2.4 | 3.2 | | | | | V |
| | | $I_{OH}$ = −6.5 mA | | | | 2.4 | 3.2 | | V |

**Note 1:** These limits apply over the entire operating range unless stated otherwise. All typical values are for $V_{CC}$ = 5.0V and $T_A$ = 25°C.

**Note 2:** During $I_{OS}$ measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

## AC Electrical Characteristics with Standard Load and Operating Conditions

**COMMERCIAL TEMP RANGE** (0°C to +70°C)

| Symbol | JEDEC Symbol | Parameter | DM74S573 | | | DM74S573A | | | DM74S573B | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| TAA | TAVQV | Address Access Time | | 40 | 60 | | 25 | 45 | | 25 | 35 | ns |
| TEA | TEVQV | Enable Access Time | | 20 | 35 | | 15 | 25 | | 15 | 25 | ns |
| TER | TEXQX | Enable Recovery Time | | 20 | 35 | | 15 | 25 | | 15 | 25 | ns |
| TZX | TEVQX | Output Enable Time | | 20 | 35 | | 15 | 25 | | 15 | 25 | ns |
| TXZ | TEXQZ | Output Disable Time | | 20 | 35 | | 15 | 25 | | 15 | 25 | ns |

**MILITARY TEMP RANGE** (−55°C to +125°C)

| Symbol | JEDEC Symbol | Parameter | DM54S573 | | | DM54S573A | | | DM54S573B | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| TAA | TAVQV | Address Access Time | | 40 | 75 | | 25 | 60 | | 25 | 50 | ns |
| TEA | TEVQV | Enable Access Time | | 20 | 45 | | 15 | 35 | | 15 | 35 | ns |
| TER | TEXQX | Enable Recovery Time | | 20 | 45 | | 15 | 35 | | 15 | 35 | ns |
| TZX | TEVQX | Output Enable Time | | 20 | 45 | | 15 | 35 | | 15 | 35 | ns |
| TXZ | TEXQZ | Output Disable Time | | 20 | 45 | | 15 | 35 | | 15 | 35 | ns |

## Functional Description

### TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

### RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

### TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of $V_{CC}$ and temperature.