



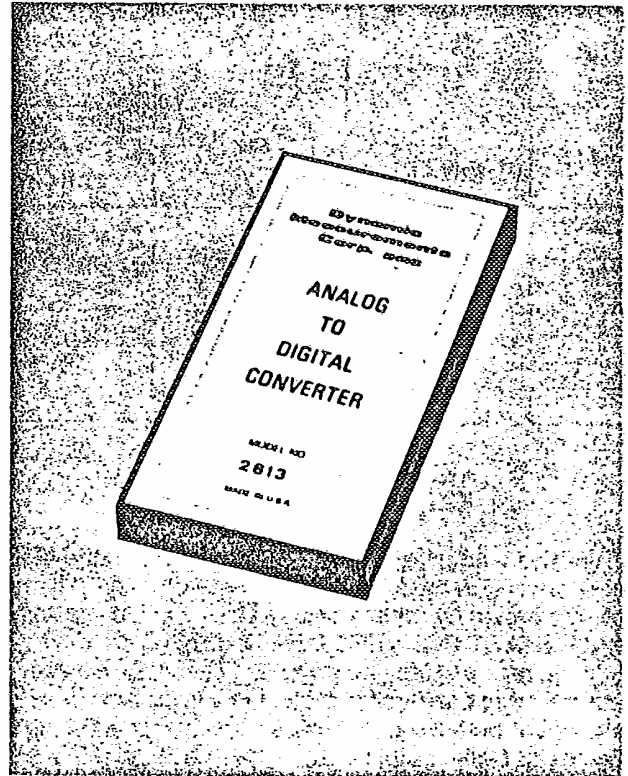
ANALOG TO DIGITAL CONVERTERS

HIGH SPEED MODELS

MAX. TOTAL CONVERSION TIMES DOWN TO:

750ns	8 Bits
1us	10 Bits
2us	12 Bits

- THROUGHPUT RATES TO 1.33MHz
- 1/4 LSB TYP. DIFFERENTIAL NONLINEARITY
- FIVE SIDES RFI/EMI SHIELDING ON 750ns AND 1μS MODELS
- LESS THAN 1/5 LSB OF NOISE TYP. AT MAJOR TRANSITIONS
- PROPRIETARY DMC CIRCUITRY PROVIDES SUPERIOR (PIN-COMPATIBLE) PERFORMANCE IN DATEL ADC-G, H AND TELEDYNE PHILBRICK 4130-4133 SLOTS



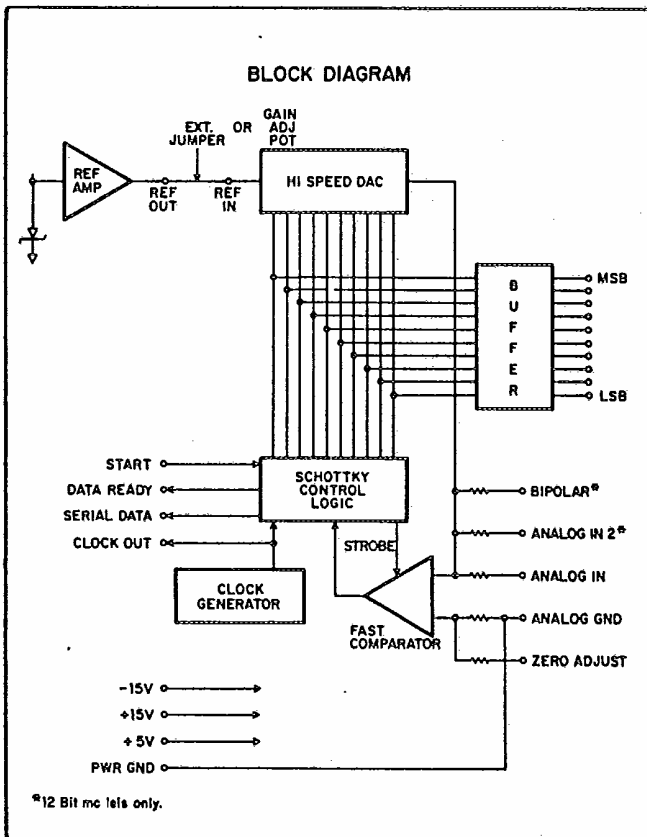
12 BIT MODELS 2809-2813

10 BIT MODELS 2800-2803

8 BIT MODELS 2804-2807

These converters are designed and characterized for use in high speed data acquisition systems, fast Fourier transform analysis, radar pulse analysis, scanning medical instrumentation and similar applications requiring fast conversion rates, good linearity and excellent stability . . . or where many inputs must be digitized in a very short period of time.

This design uses the successive approximation technique. There is an internal -10V reference, with capability for an external reference between -9V and -11V. The digital outputs are fully buffered to eliminate loading problems that could affect accuracy. Precision metal film technology is employed for ultra-stable operation.



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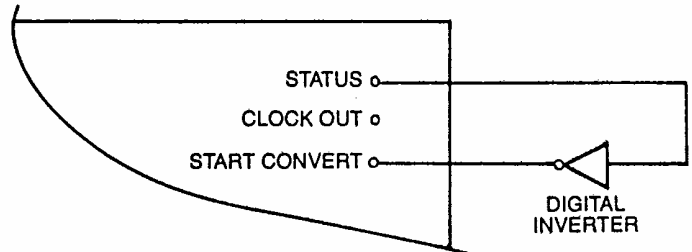
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Model	Resolution	Max. Total Conversion Time	Min. Throughput Rate	Bipolar Input Ranges	Unipolar Input Ranges	Input Resistance	Model
2809	12 bits	2us	0.500MHz	±5V	0 to -10V	1KΩ±0.5%	2809
				±10V	0 to -20V	2KΩ±0.5%	
2811		2.5us	0.400MHz	±5V	0 to -10V	1KΩ±0.5%	2811
				±10V	0 to -20V	2KΩ±0.5%	
2813		4us	0.250MHz	±5V	0 to -10V	1KΩ±0.5%	2813
				±10V	0 to -20V	2KΩ±0.5%	
2800	10 bits	1us	1MHz		0 to -5V	0.5KΩ±3Ω	2800
2801					0 to -10V	1KΩ±5Ω	2801
2802				±5V		1KΩ±5Ω	2802
2803				±10V		2KΩ±10Ω	2803
2804	8 bits	750ns	1.333MHz		0 to -5V	0.5KΩ±3Ω	2804
2805					0 to -10V	1KΩ±5Ω	2805
2806				±5V		1KΩ±5Ω	2806
2807				±10V		2KΩ±10Ω	2807

CONVERSION MODES . . . REPETITIVE AND SINGLE

These converters are designed to be used in the single conversion mode, where the user controls the rate of conversion by means of an external pulse applied to the START CONVERT input. A +5V pulse of 50nsec min. to 150nsec max. (2 TTL loads) will initiate a 1 usec conversion cycle. Data valid time is shown for both serial and parallel data in the Timing Diagram. Serial output data is made available in a nonreturn to zero (NRZ) format with the MSB occurring first.

Repetitive operation can be achieved by using a digital inverter, but the inverter delay must be added to the total conversion time. The table gives examples of the delays encountered with the more popular digital inverters.

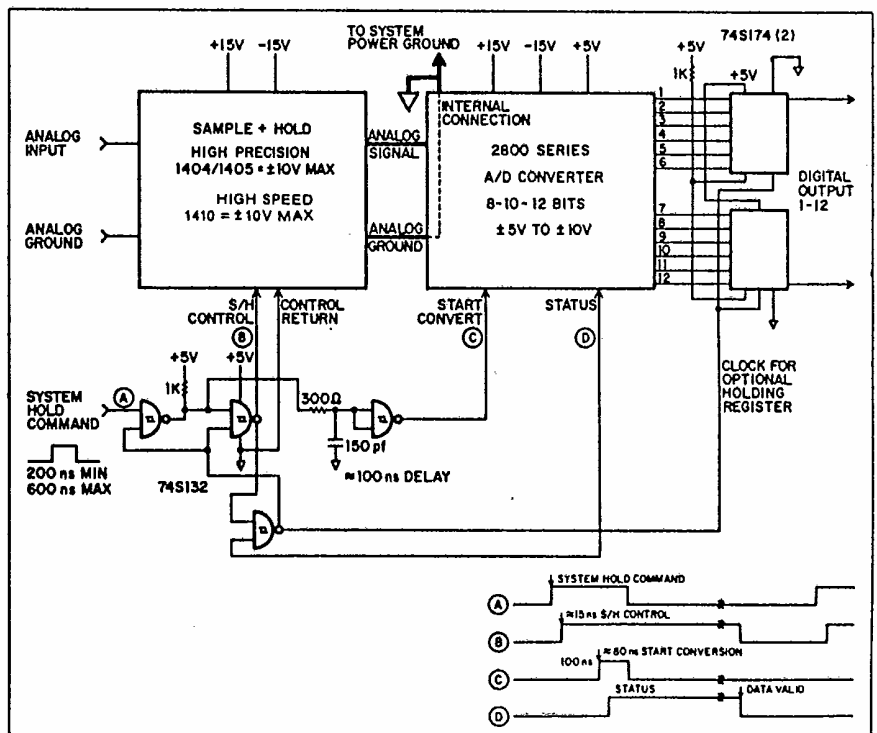


Delay In nsec		
Type	Typical	Max.
7404	12	22
74H04	6	10
74S04	3	4.5
74L04	35	60
74LS04	9	15

TYPICAL SYSTEM FOR CONVERTING FAST MOVING ANALOG SIGNALS

With conventional circuitry and converters it has often been difficult to work with analog signals which move more than 1/2 LSB during conversion. This approach achieves practical system throughput rates up to 1MHz . . . using a sample and hold amplifier from the DMC Model 1400 family in conjunction with one of these ultra-high speed A/D converters.

A single 74S132 provides proper timing for the switching glitch to settle when going into "hold" before starting the A/D conversion. The "hold" command is switched to "sample" upon conversion completion . . . allowing maximum time to reacquire the next analog level.

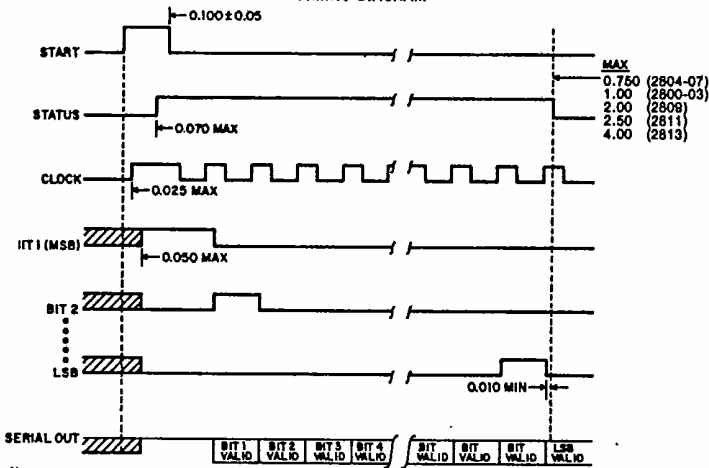


OPERATING SPECIFICATIONS
 Typical and nominal at +25°C, unless otherwise noted
 Minimum warmup time 10 minutes

Group	Item	12 Bit Models 2809-13	10 Bit Models 2800-03	8 Bit Models 2804-07
INPUTS	Digital Inputs Initiate Conversion Pulse Width Maximum Input Loading Reference Input	TTL Positive Pulse 100ns±50ns 1 TTL Load -10V, 4KΩ		
	Input Power	+15V±0.5V @ 50mA max. -15V±0.5V @ 30mA max. +5V±0.25V @ 325mA max.	+15V±0.5V @ 40mA max. -15V±0.5V @ 30mA max. +5V±0.25V @ 325mA max.	+15V±0.5V @ 40mA max. -15V±0.5V @ 30mA max. +5V±0.25V @ 325mA max.
CHARACTERISTICS	Accuracy Nonlinearity	±½ LSB max. ±½ LSB max.		
	Differential Nonlinearity Zero Offset Error ① Gain Error ①	±10mV ±0.1% max.	±10mV ±0.06% typ., ±0.1% max.	±25mV ±0.2% typ., ±0.3% max.
TRANSFER	Stability vs. Temperature Nonlinearity	±5ppm/°C max.	±10ppm/°C max.	±10ppm/°C max.
	Differential Nonlinearity Zero Offset Error	±3ppm/°C typ., ±5ppm/°C max.	±5ppm/°C typ., ±10ppm/°C max.	±5ppm/°C typ., ±10ppm/°C max.
	Unipolar	±5ppm/°C max.	±15ppm/°C max.	±15ppm/°C max.
	Bipolar	±10ppm/°C max.	±15ppm/°C max.	±15ppm/°C max.
	Gain Error	±10ppm/°C max.	±10ppm/°C max.	±20ppm/°C max.
	Conversion Time	+2.8ns/°C max.	+2ns/°C max.	+2ns/°C max.
	Vref out		±3ppm/°C typ., ±10ppm/°C max.	
	Long-Term Stability	0.007%/month	0.01%/month	0.02%/month
	3σ Noise, P-P	0.01% FS	0.02% FS	0.02% FS
	PSRR (Ref to Input)		0.002%/%	
OUTPUTS	Reference Output (-5mA)	-10V±0.1%	-10V±0.1%	-10V±1.0%
	Digital Outputs Logic Codes Parallel Unipolar Parallel Bipolar Serial Unipolar Serial Bipolar Format Output Drive, Min. Switching Levels "0" State "1" State Status "1" State Output Drive, Min. Clock Out Logic Output Drive, Min. Pulse Width		BIN OBIN, 2's C BIN OBIN NRZ 8 TTL Loads	
	"0" State		≤0.5V	
	"1" State		≥2.4V	
	5 TTL Loads		During Conversion 5 TTL Loads	4 TTL Loads
			TTL Positive Pulse 8 TTL Loads 40ns	
ENVIRONMENTAL	Temperature Ranges Operating, Full Ratings Operating, 50% Derated Storage	0°C to +70°C -25°C to +85°C -55°C to +125°C		
	Relative Humidity Shielding	95% Non-condensing RFI and EMI, on five sides		
RATINGS	Absolute Maximum Ratings Supply Voltage to Ground ±15V Input +5V Input Digital Input Voltage Analog Input Voltage Rin = 250Ω Rin = 500Ω Rin = 1KΩ Rin = 2KΩ	±8V	±18V +6V +5V ±11V ±16V ±22V	

Notes: ① Adjustable to Zero

TIMING DIAGRAM



- Notes:
 1. All times are shown in microseconds.
 2. Indicated bit states assume digital outputs are all 0's.
 3. indicates unknown state.

DIGITAL CODES

Analog Input	UNIPOLAR	BIPOLAR	
	Binary	Offset Binary	2's Complement
+FS		000 000	100 000
+FS-1 LSB		000 001	100 001
+3/4 Scale		001 000	101 000
+1/2 Scale		010 000	110 000
0+1 LSB		011 111	111 111
0	000 000	100 000	000 000
0-1 LSB	000 001	100 001	000 001
-1/2 Scale	100 000	110 000	010 000
-3/4 Scale	110 000	111 000	011 000
-FS+1 LSB	111 111	111 111	011 111

GAIN TRIMMING

All models are gain-trimmed by DMC to within 1/2 LSB of specified full scale input voltage. For optional gain trimming, apply -FS+1 1/2 LSB of voltage to ANALOG INPUT*. With the gain trim potentiometer, set the digital output exactly on the threshold of changing from 111 . . . 110 to 111 . . . 111.

OFFSET TRIMMING

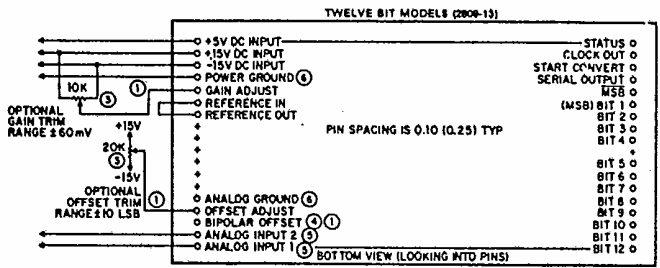
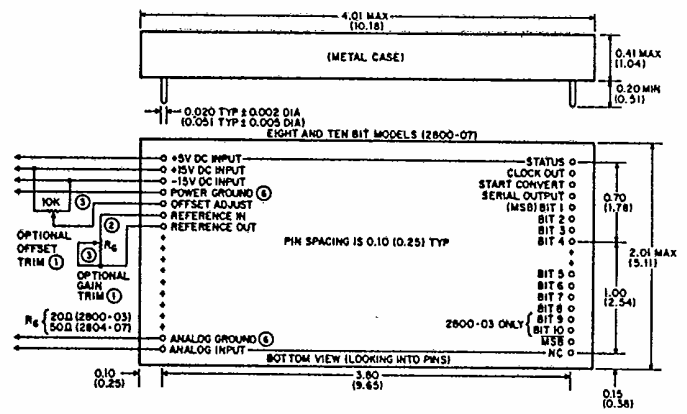
Apply -1/2 LSB (for unipolar mode) or +FS-1/2 LSB (for bipolar mode) of voltage to ANALOG INPUT*. With the offset trim potentiometer, set the digital output exactly on the threshold of changing from all 0's to 000 . . . 001.

*Twelve-bit models (2809-13) have two ANALOG INPUTS. Trimming either one will automatically trim the other.

POWER AND GROUNDING CONSIDERATIONS IN HIGH SPEED SYSTEMS

For maximum accuracy and speed, high speed systems require added care in power distribution. To minimize RF contamination, supply voltages should be bussed. For optimum performance, it is good practice to bypass each power supply input with a 1uF tantalum capacitor and a 0.01uF disc capacitor.

To guard against ground loop errors, the system power ground must be at very low impedance . . . since ANALOG GROUND is internally connected to POWER GROUND.



CONNECTION NOTES:

- ① Pins are left unconnected when optional trim circuits are not used. Please see Note ②
- ② On eight and ten bit models (2800-07) when optional gain trim is not used, please connect REFERENCE OUT to REFERENCE IN, unless an external reference is used.
- ③ Potentiometers should be Cermet ($\leq 100\text{ppm}/^\circ\text{C}$).
- ④ For bipolar operation of twelve bit models (2809-13), please connect BIPOLAR OFFSET to REFERENCE OUT.
- ⑤ To select input voltage ranges on twelve bit models, please use ANALOG INPUT 1 for -2.5V/ $\pm 1.25\text{V}$ ranges and also for -10V/ $\pm 5\text{V}$ ranges. Please use ANALOG INPUT 2 for -5V/ $\pm 2.5\text{V}$ ranges and also for -20V/ $\pm 10\text{V}$ ranges.
- ⑥ POWER GROUND and ANALOG GROUND are internally connected.

MECHANICAL NOTES:

7. Dimensions in parentheses are in Centimeters.
8. Dimensional tolerance between pins is ± 0.01 (± 0.025), non-cumulative. Dimensional tolerance from case edge to center of pins is ± 0.02 (± 0.51).
9. DMC Mating Socket is Model 6524 (2 req'd.)

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