ALDEC 8243 IP Core Data Sheet

Overview

The 8243 core is the HDL model of the Intel™ 8243 input/output expander

Features

- Functionally based on the Intel 8243 device
- Five 4-bit peripheral ports: P20, P40, P50, P60, P70
- Two control signals: CS, PROG
- Four programming modes for peripherals (three write and read modes)
- 4-bit bidirectional system data bus with standard microprocessor interface controls

Pinout

Table 1: **Core Signal Pinout**

Name	Direction	Description
PROG	Input	Clock input. A high-to-low transition on the PROG input signifies that the address and control bits are available on the P20 port, and a low-to-high transition signifies that data are available on the P20 port.
nCS	Input	Chip select input. A high on the CS input inhibits any changes of the output signals or the internal status.
P20[3:0] [1)]	Bidirectional	4-bit bidirectional port contains the address and control bits on a high-to-low transition of the PROG input. During a low-to-high transition, the port contains data for a selected output port during the write operation, or the data from a selected port before the low-to-high transition during the read operation.
P40[3:0] [1)] P50[3:0] P60[3:0] P70[3:0]	Bidirectional	4-bit bidirectional I/O ports. Could be programmed as the input (during the read operation), low impedance latched output (after the write operstion), or the tri-state (after the read operation). Data on pins P20-P23 could be written directly or logically mixed with previous data (AND or OR logic).

Notes:

1) Each bidirectional pin is defined in the core interface as three separated ports. Optionally, using the HDL Interface, it can be merged to one bidirectional HDL port.

Block Diagram

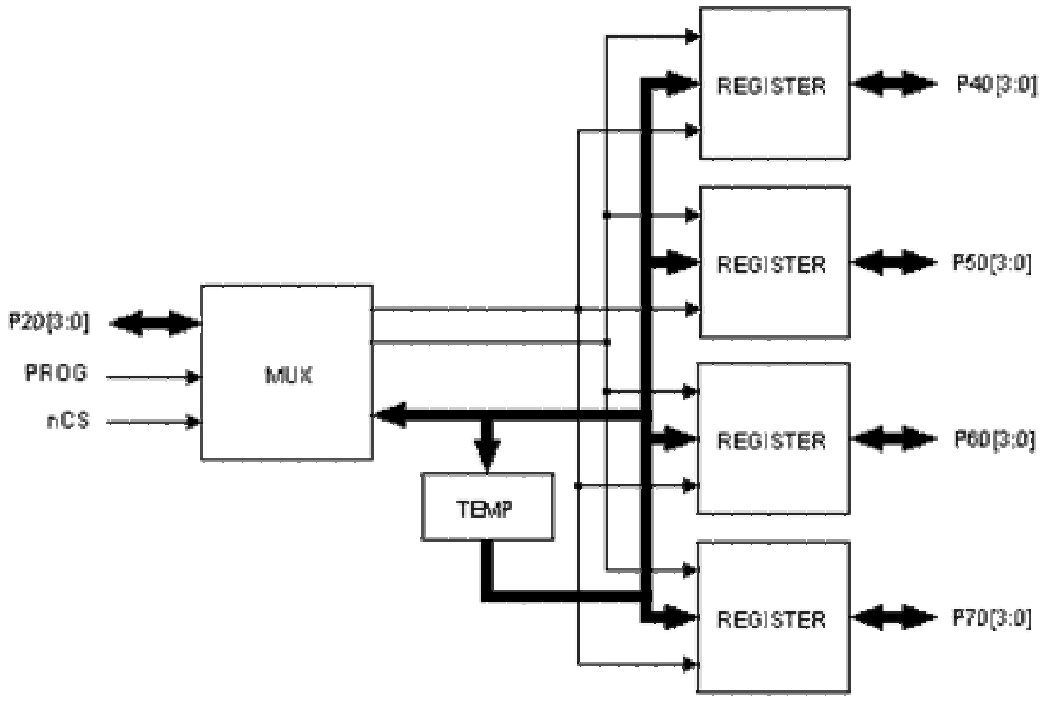

Figure 1: **Core Structure**

Deliverables

Available at No Cost:

- Verilog and/or VHDL Simulation Model (Encrypted for Aldec simulator only)
- Data Sheet
- Application Notes

Available Upon ordering:

- VHDL/Verilog source code
- Technology-dependent EDIF and VHDL/Verilog netlists
- Verification Test Bench source code
- RTL Source compilation and simulation scripts
- Synthesis scripts
- User-Guide

Ordering Information

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