CA3401

Quad Single-Supply Operational Amplifier

For Automotive Electronics and Industrial Control Systems

Features:

- *Single-supply operation – +5 V to +18 Vdc*
- *Internally compensated*
- *Wide unity-gain bandwidth – 5 MHz typ.*
- *Low input bias current – 50 nA typ.*
- *High open-loop gain – 2000 V/V typ.*

The RCA-3401 is a high-gain monolithic quad operational amplifier designed specifically for applications using a single positive power supply. No external compensation is necessary. Closed-loop stability in each of the four independent amplifiers is maintained by a 3-pF on-chip capacitor. The CA3401 is ideally suited for applications in industrial control systems, automotive electronics, and general purpose amplifiers, e.g. oscillators, tachometers, active filters, and multichannel amplifiers.

The CA3401 is supplied in a 14-lead dual-in-line plastic package (E suffix), and is also available in chip form (H suffix). It is a direct replacement for the Motorola MC3401P, and is pin-compatible with the Motorola MC3301P and the National Semi-conductor LM3900N. The CA3401 can be operated over the temperature range of -55 to +125°C, although the limit values of certain specified electrical characteristics apply only over the range of 0 to +75° C.

Applications:

- *Automotive*
- *Constant-Current Sources*
- *Multivibrators*
- *Sample and Hold*
- *Square-Wave Generator*
- *Oscillators*
- *Tachometers*
- *Active Filters*
- *Multi-Channel Amplifiers*
- *Summing Amplifiers*

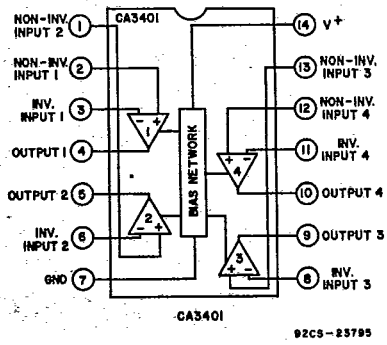


Fig. 1 – Block diagram of CA3401.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

DC SUPPLY VOLTAGE	+18 V
INPUT SIGNAL CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25° C	625 mW
Above T_A = 25° C	Derate lineary 5 mW/° C
AMBIENT TEMPERATURE RANGE:	
Operating	-55 to + 125° C
Storage	-65 to + 150° C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	300° C

File Number **630**

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V^+ = 15$ V (Unless Indicated Otherwise)

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
STATIC					
Output Voltage: High, V_{OH}		13.5	14.2	–	V
Low, V_{OL}		–	0.03	0.1	
Max. Undistorted Output Swing, V_{OP-P}	$0^oC<T_A<75^oC$	10	13.5	–	
Output Current: Source, I_{SOURCE}		5	10	–	mA
Sink, I_{SINK}		0.5	1	–	
Total Quiescent Current: I_Q Noninverting inputs open		–	6.9	10	mA
Noninverting inputs grounded		–	7.8	14	
Input Bias Current, I_{IB}	$R_L = \infty$ $T_A = 25^oC$	–	50	300	nA
	$R_L = \infty$ $0^oC \leq T_A \leq 75^oC$	–	–	500	
DYNAMIC					
Open-Loop Voltage Gain, A_{OL}	$T_A = 25^oC$	1000	2000	–	V/V
	$0^oC \leq T_A \leq 75^oC$	800	–	–	
Input Resistance, R_I		0.1	1	–	MΩ
Slew Rate, SR	$C_L = 100$ pF, $R_L = 5$ kΩ	–	0.6	–	V/μs
Unity Gain Gandwidth, BW		–	5	–	MHz
Phase Margin, ϕ		–	70	–	Degrees
Power Supply Rejection	f = 100 Hz	–	55	–	dB
Channel Separation, e_{01}/e_{02}	f = 1 kHz	–	65	–	dB

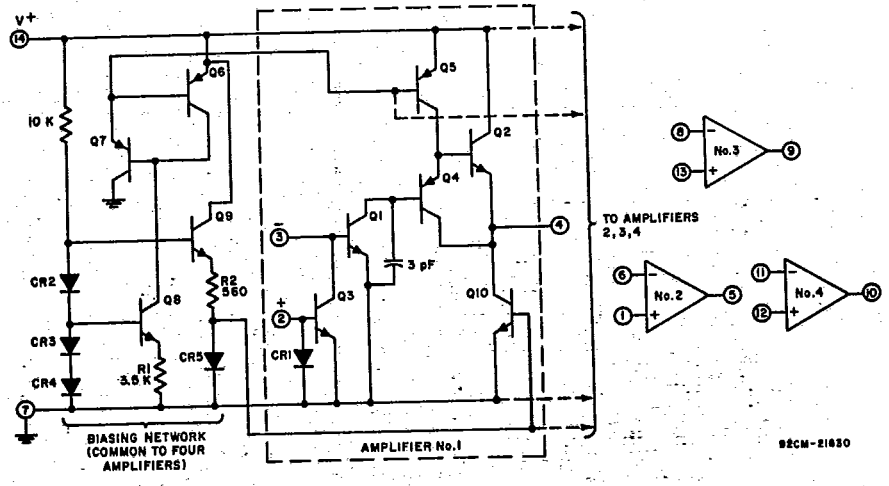


Fig.2 – Schematic diagram of CA3401.

CA3401

TEST CIRCUITS

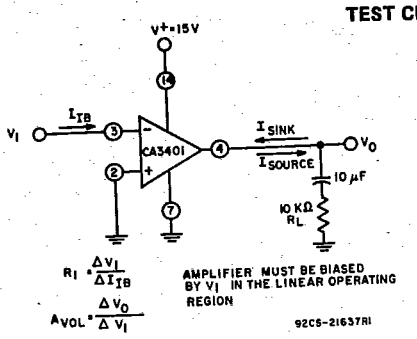


Fig.3 – Open-loop gain and input resistance, input bias current and output current test circuit.

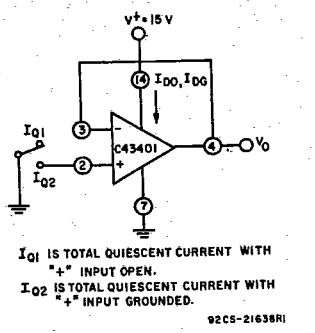


Fig.4 – Quiescent power supply current test circuit.

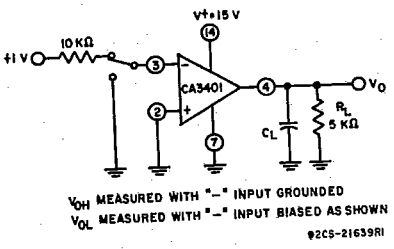


Fig.5 – Output voltage swing test circuit.

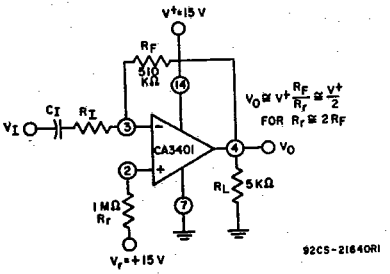


Fig.6 – Peak-to-peak output voltage test circuit.

TYPICAL CHARACTERISTIC CURVES

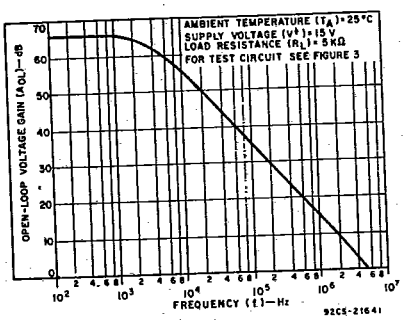


Fig.7 – Open-loop voltage gain vs. frequency.

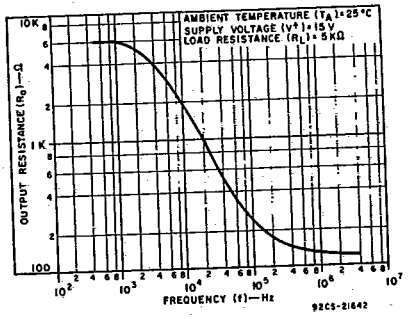


Fig.8 – Output resistance vs. frequency.

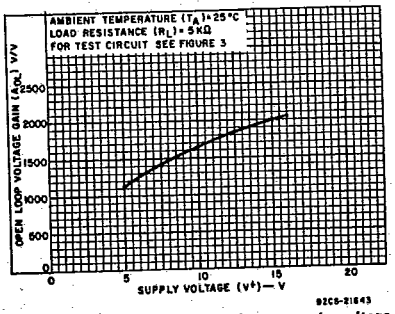


Fig.9 – Open-loop voltage gain vs. supply voltage.

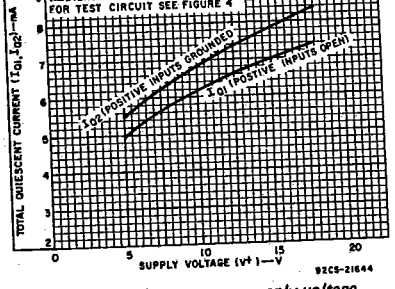


Fig.10 – Supply current vs. supply voltage.

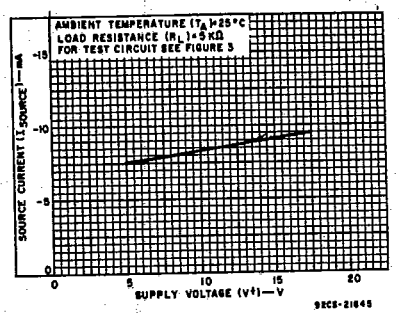


Fig.11 – Source current vs. supply voltage.

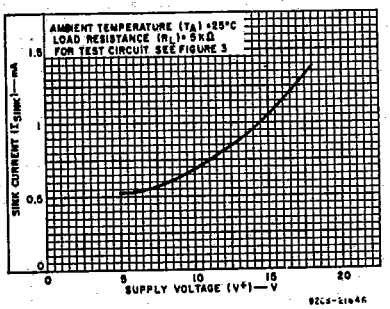
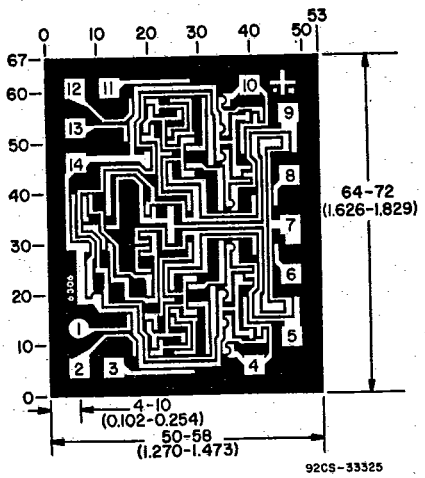


Fig.12 – Sink current vs. supply voltage.



Dimensions and pad layout for CA3401H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.