National Semiconductor

May 1999

LM6172
Dual High Speed, Low Power, Low Distortion, Voltage Feedback Amplifiers

General Description

The LM6172 is a dual high speed voltage feedback amplifier. It is unity-gain stable and provides excellent DC and AC performance. With 100 MHz unity-gain bandwidth, 3000V/µs slew rate and 50 mA of output current per channel, the LM6172 offers high performance in dual amplifiers; yet it only consumes 2.3 mA of supply current each channel.

The LM6172 operates on ±15V power supply for systems requiring large voltage swings, such as ADSL, scanners and ultrasound equipment. It is also specified at ±5V power supply for low voltage applications such as portable video systems.

The LM6172 is built with National's advanced VIP™ III (Vertically Integrated PNP) complementary bipolar process. See the LM6171 datasheet for a single amplifier with these same features.

Features

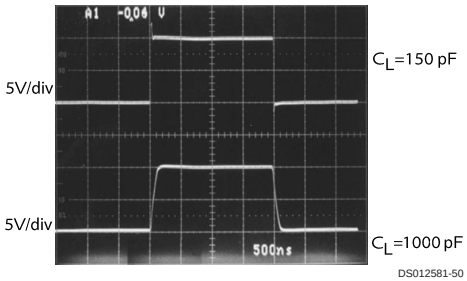
(Typical Unless Otherwise Noted)

- Easy to Use Voltage Feedback Topology
- High Slew Rate 3000V/µs
- Wide Unity-Gain Bandwidth 100 MHz
- Low Supply Current 2.3 mA/Channel
- High Output Current 50 mA/channel
- Specified for ±15V and ±5V Operation

Applications

- Scanner I-to-V Converters
- ADSL/HDSL Drivers
- Multimedia Broadcast Systems
- Video Amplifiers
- NTSC, PAL® and SECAM Systems
- ADC/DAC Buffers
- Pulse Amplifiers and Peak Detectors

LM6172 Driving Capacitive Load



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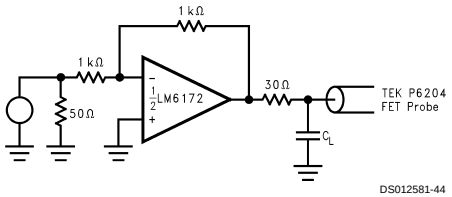

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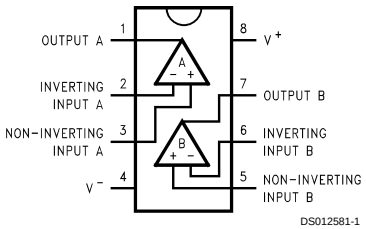
Connection Diagram

8-Pin DIP/SO



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Top View

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Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C	Military −55˚C to +125˚C		
8-Pin DIP	LM6172IN		Rails	N08E
8-Pin CDIP	LM6172AMJ-QML	5962-95604	Rails	J08A
10-Pin Ceramic SOIC	LM6172AMWG-QML	5962-95604	Trays	WG10A
8-Pin Small Outline	LM6172IM		Rails	M08A
	LM6172IMX		Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	3 kV
Machine Model	300V
Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 9)	±10V
Output Short Circuit to Ground (Note 3)	Continuous
Storage Temp. Range	−65˚C to +150˚C
Maximum Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	$5.5V \le V_S \le 36V$
Junction Temperature Range	
LM6172I	$-40˚C \le T_J \le +85˚C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	95˚C/W
M Package, 8-Pin Surface Mount	160˚C/W

±15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C,V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6172I Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		0.4	3	mV
				4	max
TC V_{OS}	Input Offset Voltage Average Drift		6		µV/˚C
I_B	Input Bias Current		1.2	3	µA
				4	max
I_{OS}	Input Offset Current		0.02	2	µA
				3	max
R_{IN}	Input Resistance	Common Mode	40		MΩ
		Differential Mode	4.9		
R_O	Open Loop Output Resistance		14		Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	110	70	dB
				65	min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	95	75	dB
				70	min
A_V	Large Signal Voltage Gain (Note 6)	R_L = 1 kΩ	86	80	dB
				75	min
		R_L = 100Ω	78	65	dB
				60	min
V_O	Output Swing	R_L = 1 kΩ	13.2	12.5	V
				12	min
			−13.1	−12.5	V
				−12	max
		R_L = 100Ω	9	6	V
				5	min
			−8.5	−6	V
				−5	max
	Continuous Output Current (Open Loop) (Note 7)	Sourcing, R_L = 100Ω	90	60	mA
				50	min
		Sinking, R_L = 100Ω	−85	−60	mA
				−50	max
I_{SC}	Output Short Circuit Current	Sourcing	107		mA
		Sinking	−105		mA
I_S	Supply Current	Both Amplifiers	4.6	8	mA

±15V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C,V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6172I Limit (Note 5)	Units
				9	max

±15V AC Electrical Characteristics

Unless otherwise specified, T_J = 25˚C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ

Symbol	Parameter	Conditions	LM6172I Typ (Note 5)	Units
SR	Slew Rate	A_V = +2, V_{IN} = 13 V_{PP}	3000	V/µs
		A_V = +2, V_{IN} = 10 V_{PP}	2500	V/µs
	Unity-Gain Bandwidth		100	MHz
	−3 dB Frequency	A_V = +1	160	MHz
		A_V = +2	62	MHz
	Bandwidth Matching between Channels		2	MHz
ϕ_m	Phase Margin		40	Deg
t_s	Settling Time (0.1%)	A_V = −1, V_{OUT} = ±5V, R_L = 500Ω	65	ns
A_D	Differential Gain (Note 8)		0.28	%
ϕ_D	Differential Phase (Note 8)		0.6	Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	12	$\frac{pA}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	1	$\frac{nV}{\sqrt{Hz}}$
	Second Harmonic Distortion (Note 10)	f = 10 kHz	−110	dB
		f = 5 MHz	−50	dB
	Third Harmonic Distortion (Note 10)	f = 10 kHz	−105	dB
		f = 5 MHz	−50	dB

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6172I Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		0.1	3 **4**	mV max
TC V_{OS}	Input Offset Voltage Average Drift		4		µV/˚C
I_B	Input Bias Current		1.4	2.5 **3.5**	µA max
I_{OS}	Input Offset Current		0.02	1.5 **2.2**	µA max
R_{IN}	Input Resistance	Common Mode	40		MΩ
		Differential Mode	4.9		
R_O	Output Resistance		14		Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	105	70	dB

±5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6172I Limit (Note 5)	Units
				65	min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	95	75	dB
				70	min
A_V	Large Signal Voltage Gain (Note 6)	R_L = 1 kΩ	82	70	dB
				65	min
		R_L = 100Ω	78	65	dB
				60	min
V_O	Output Swing	R_L = 1 kΩ	3.4	3.1	V
				3	min
			−3.3	−3.1	V
				−3	max
		R_L = 100Ω	2.9	2.5	V
				2.4	min
			−2.7	−2.4	V
				−2.3	max
	Continuous Output Current (Open Loop) (Note 7)	Sourcing, R_L = 100Ω	29	25	mA
				24	min
		Sinking, R_L = 100Ω	−27	−24	mA
				−23	max
I_{SC}	Output Short Circuit Current	Sourcing	93		mA
		Sinking	−72		mA
I_S	Supply Current	Both Amplifiers	4.4	6	mA
				7	max

±5V AC Electrical Characteristics

Unless otherwise specified, T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ.

Symbol	Parameter	Conditions	LM61722 Typ (Note 5)	Units
SR	Slew Rate	A_V = +2, V_{IN} = 3.5 V_{PP}	750	V/µs
	Unity-Gain Bandwidth		70	MHz
	−3 dB Frequency	A_V = +1	130	MHz
		A_V = +2	45	MHz
ϕ_m	Phase Margin		57	Deg
t_s	Settling Time (0.1%)	A_V = −1, V_{OUT} = ±1V, R_L = 500Ω	72	ns
A_D	Differential Gain (Note 8)		0.4	%
ϕ_D	Differential Phase (Note 8)		0.7	Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz	11	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	1	$\frac{pA}{\sqrt{Hz}}$
	Second Harmonic Distortion (Note 10)	f = 10 kHz	−110	dB
		f = 5 MHz	−48	dB
	Third Harmonic	f = 10 kHz	−105	dB

±5V AC Electrical Characteristics (Continued)

Unless otherwise specified, T_J = 25˚C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ.

Symbol	Parameter	Conditions	LM61722 Typ (Note 5)	Units
	Distortion (Note 10)	f = 5 MHz	−50	dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine Model, 200Ω in series with 100 pF.

Note 3: Continuous short circuit operation can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.

Note 8: The open loop output current is the output swing with the 100Ω load resistor divided by that resistor.

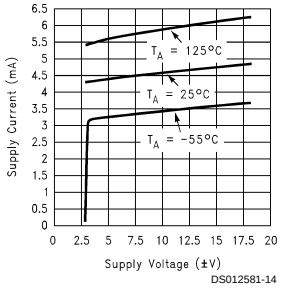
Note 9: Differential gain and phase are measured with A_V = +2, V_{IN} = 1 V_{PP} at 3.58 MHz and both input and output 75Ω terminated.

Note 10: Differential input voltage is applied at V_S = ±15V.

Note 11: Harmonics are measured with A_V = +2, V_{IN} = 1 V_{PP} and R_L = 100Ω.

Typical Performance Characteristics unless otherwise noted, T_A = 25˚C

Supply Voltage vs Supply Current



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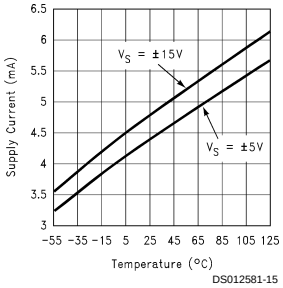
Supply Current vs Temperature



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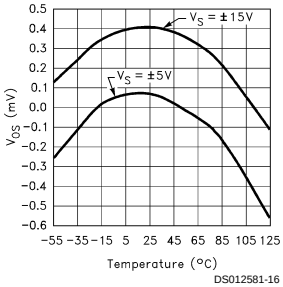
Input Offset Voltage vs Temperature



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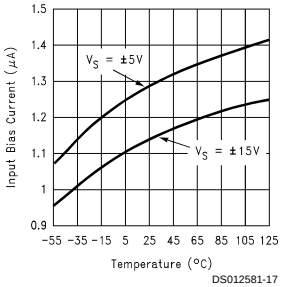
Input Bias Current vs Temperature



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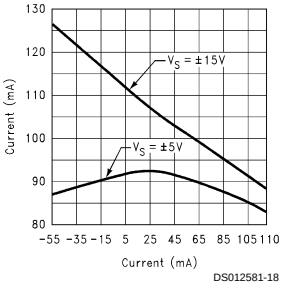
Short Circuit Current vs Temperature (Sourcing)



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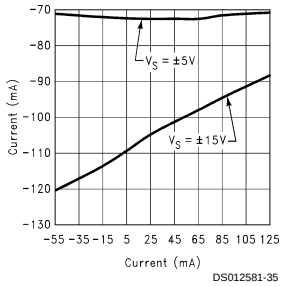
Short Circuit Current vs Temperature (Sinking)



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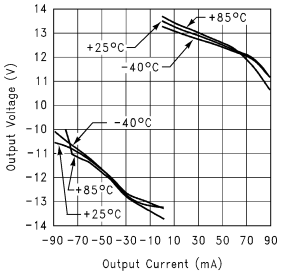
Typical Performance Characteristics unless otherwise noted, T_A = 25˚C (Continued)

Output Voltage vs Output Current (V_S = ±15V)



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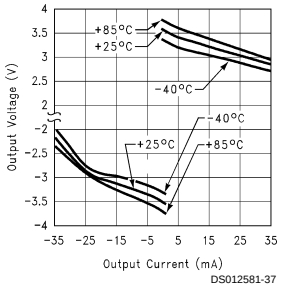
Output Voltage vs Output Current (V_S = ±5V)



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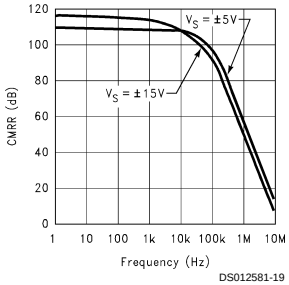
CMRR vs Frequency



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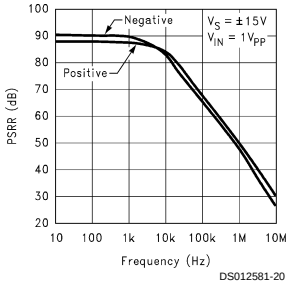
PSRR vs Frequency



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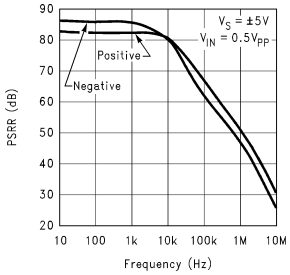
PSRR vs Frequency



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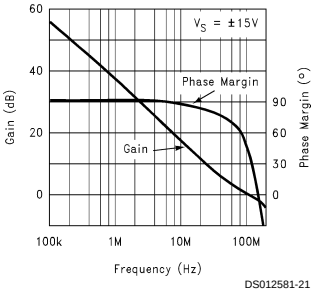
Open-Loop Frequency Response



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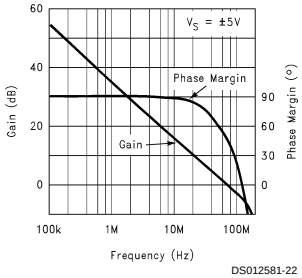
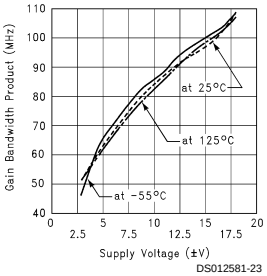
Open-Loop Frequency Response



DS012581-22

Gain-Bandwidth Product vs Supply Voltage at Different Temperature



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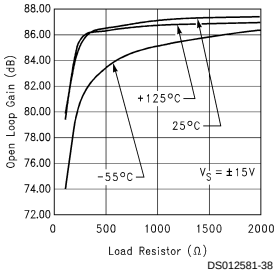
Large Signal Voltage Gain vs Load



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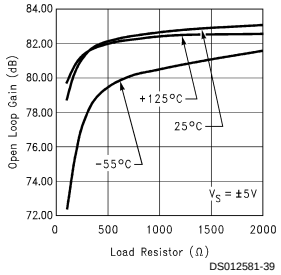
Typical Performance Characteristics unless otherwise noted, T_A = 25˚C (Continued)

Large Signal Voltage Gain vs Load



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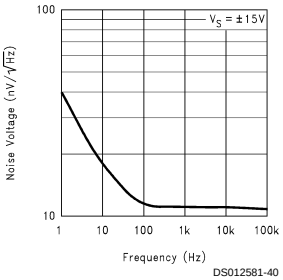
Input Voltage Noise vs Frequency



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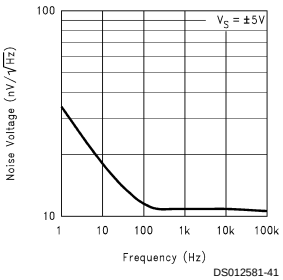
Input Voltage Noise vs Frequency



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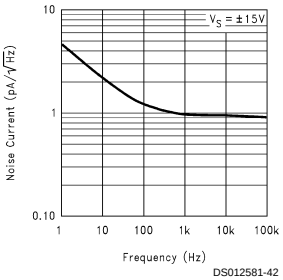
Input Current Noise vs Frequency



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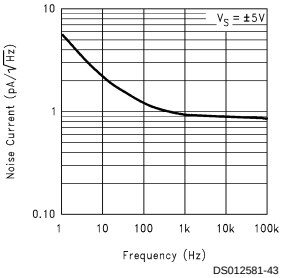
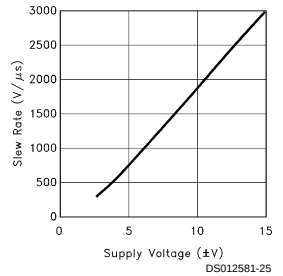
Input Current Noise vs Frequency



DS012581-43

Slew Rate vs Supply Voltage



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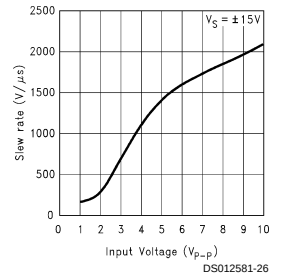
Slew Rate vs Input Voltage



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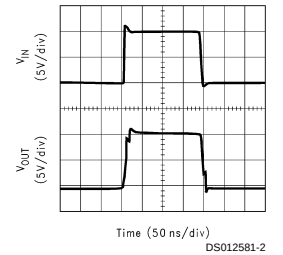
Large Signal Pulse Response A_V = +1, V_S = ±15V



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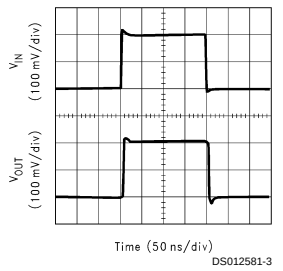
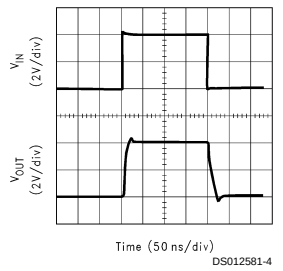
Small Signal Pulse Response A_V = +1, V_S = ±15V



DS012581-3

Large Signal Pulse Response A_V = +1, V_S = ±5V



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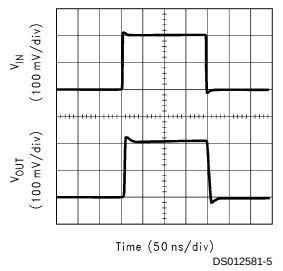
Small Signal Pulse Response A_V = +1, V_S = ±5V



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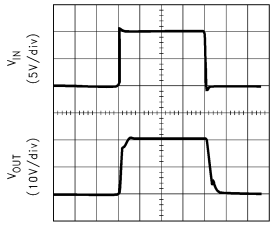
Typical Performance Characteristics unless otherwise noted, T_A = 25˚C (Continued)

Large Signal Pulse Response
A_V = +2, V_S = ±15V



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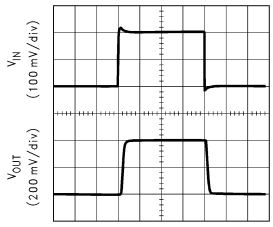
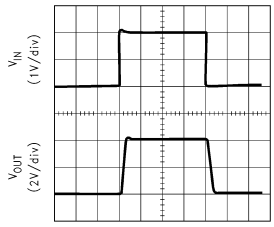
Small Signal Pulse Response
A_V = +2, V_S = ±15V



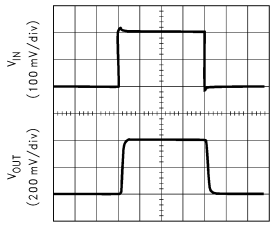
DS012581-7

Large Signal Pulse Response
A_V = +2, V_S = ±5V



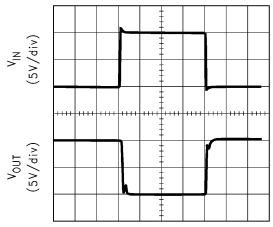
DS012581-8

Small Signal Pulse Response
A_V = +2, V_S = ±5V



DS012581-9

Large Signal Pulse Response
A_V = −1, V_S = ±15V



DS012581-10

Small Signal Pulse Response
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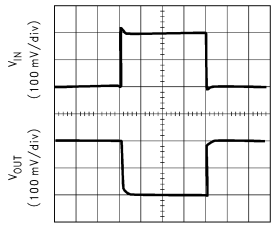

DS012581-11

Large Signal Pulse Response
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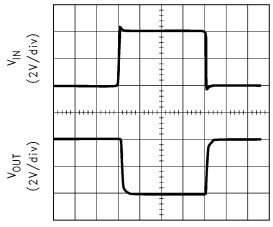
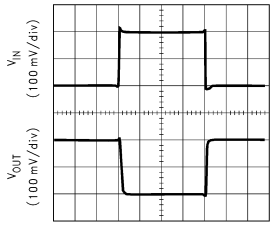


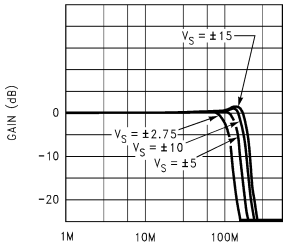
DS012581-12

Small Signal Pulse Response
A_V = −1, V_S = ±5V



DS012581-13

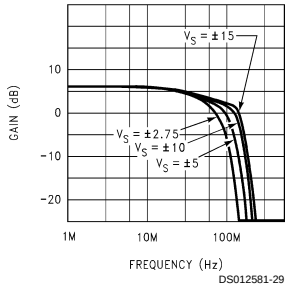
Closed Loop Frequency Response vs Supply Voltage (A_V = +1)



DS012581-28

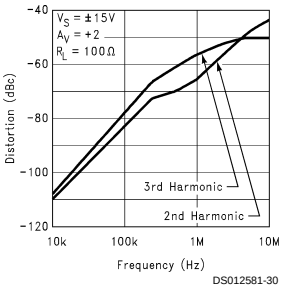
Typical Performance Characteristics unless otherwise noted, T_A = 25˚C (Continued)

Closed Loop Frequency Response vs Supply Voltage (A_V = +2)



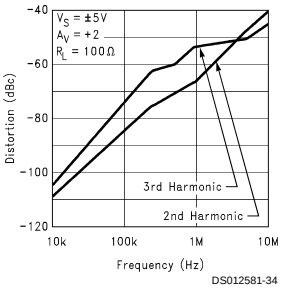
DS012581-29

Harmonic Distortion vs Frequency (V_S = ±15V)



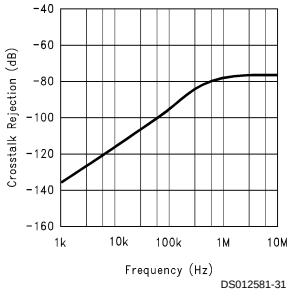
DS012581-30

Harmonic Distortion vs Frequency (V_S = ±5V)



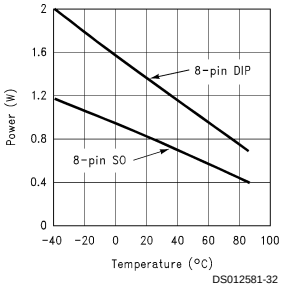
DS012581-34

Crosstalk Rejection vs Frequency



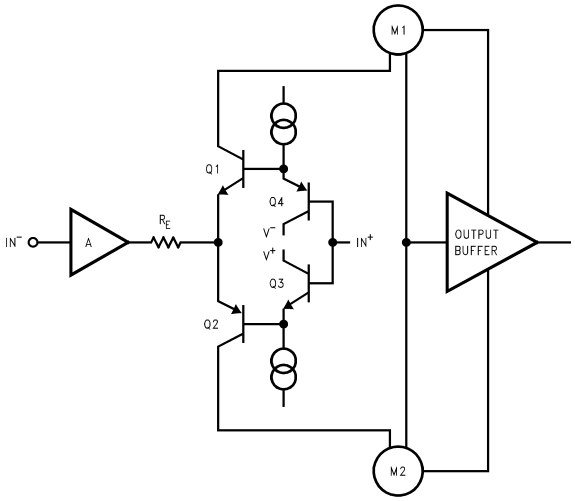
DS012581-31

Maximum Power Dissipation vs Ambient Temperature



DS012581-32

½ LM6172 Simplified Schematic



DS012581-55

Application Notes

LM6172 Performance Discussion

The LM6172 is a dual high-speed, low power, voltage feedback amplifier. It is unity-gain stable and offers outstanding performance with only 2.3 mA of supply current per channel. The combination of 100 MHz unity-gain bandwidth, 3000V/µs slew rate, 50 mA per channel output current and other attractive features makes it easy to implement the LM6172 in various applications. Quiescent power of the LM6172 is 138 mW operating at ±15V supply and 46 mW at ±5V supply.

LM6172 Circuit Operation

The class AB input stage in LM6172 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM6172 Simplified Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM6172 Slew Rate Characteristic

The slew rate of LM6172 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1 kΩ to the input of LM6172, the slew rate is reduced to help lower the overshoot, which reduces settling time.

Reducing Settling Time

The LM6172 has a very fast slew rate that causes overshoot and undershoot. To reduce settling time on LM6172, a 1 kΩ resistor can be placed in series with the input signal to decrease slew rate. A feedback capacitor can also be used to reduce overshoot and undershoot. This feedback capacitor serves as a zero to increase the stability of the amplifier circuit. A 2 pF feedback capacitor is recommended for initial evaluation. When the LM6172 is configured as a buffer, a feedback resistor of 1 kΩ must be added in parallel to the feedback capacitor.

Another possible source of overshoot and undershoot comes from capacitive load at the output. Please see the section “Driving Capacitive Loads” for more detail.

Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in *Figure 1*. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped (slow) the pulse response becomes. For LM6172, a 50Ω isolation resistor is recommended for initial evaluation.

Driving Capacitive Loads (Continued)

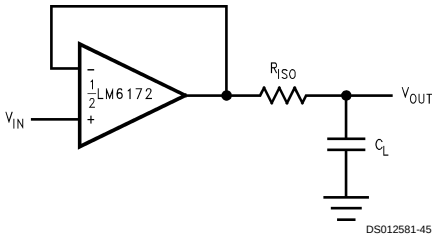


FIGURE 1. Isolation Resistor Used to Drive Capacitive Load

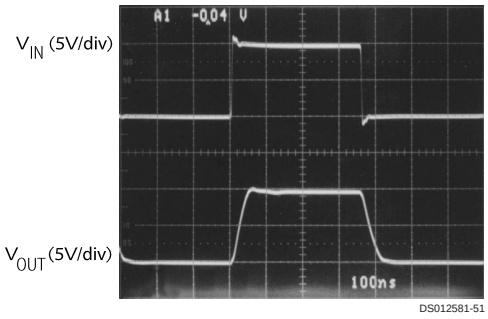


FIGURE 2. The LM6172 Driving a 510 pF Load with a 30Ω Isolation Resistor

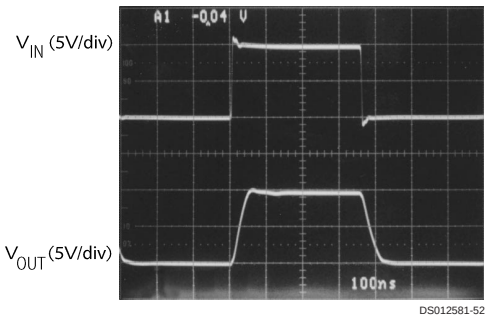


FIGURE 3. The LM6172 Driving a 220 pF Load with a 50Ω Isolation Resistor

Layout Consideration

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENTS SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM6172, a feedback resistor less than 1 kΩ gives optimal performance.

Compensation for Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F$$

can be used to cancel that pole. For LM6172, a feedback capacitor of 2 pF is recommended. *Figure 4* illustrates the compensation circuit.

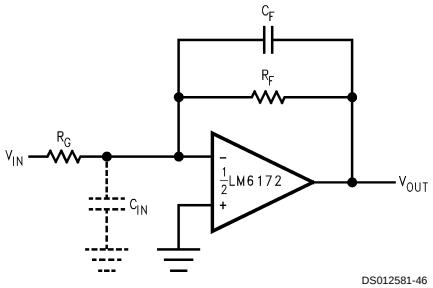


FIGURE 4. Compensating for Input Capacitance

Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 µF ceramic capacitors directly to power supply pins and 2.2 µF tantalum capacitors close to the power supply pins.

Power Supply Bypassing (Continued)

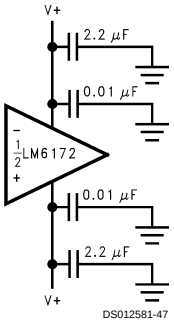


FIGURE 5. Power Supply Bypassing

Termination

In high frequency applications, reflections occur if signals are not properly terminated. *Figure 6* shows a properly terminated signal while *Figure 7* shows an improperly terminated signal.

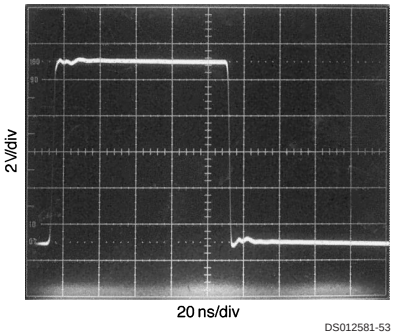


FIGURE 6. Properly Terminated Signal

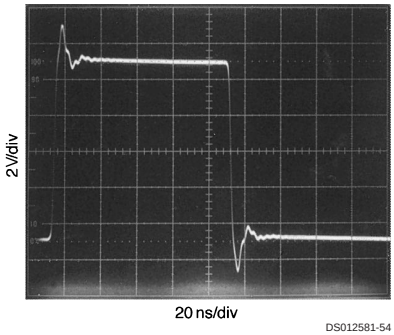


FIGURE 7. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA}$$

Where P_D is the power dissipation in a device

$T_{J(max)}$ is the maximum junction temperature

T_A is the ambient temperature

θ_{JA} is the thermal resistance of a particular package

For example, for the LM6172 in a SO-8 package, the maximum power dissipation at 25˚C ambient temperature is 780 mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (95˚C/W) than that of 8-pin SO (160˚C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

P_Q: = supply current x total supply voltage with no load

P_L: = output current x (voltage difference between supply voltage and output voltage of the same supply)

For example, the total power dissipated by the LM6172 with V_S = ±15V and both channels swinging output voltage of 10V into 1 kΩ is

P_D: = $P_Q + P_L$

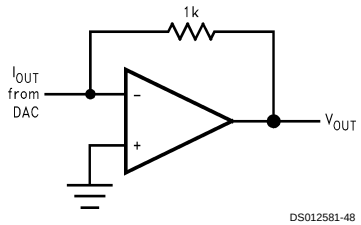
: = 2[(2.3 mA)(30V)] + 2[(10 mA)(15V − 10V)]

: = 138 mW + 100 mW

: = 238 mW

Application Circuits

I-to-V Converters



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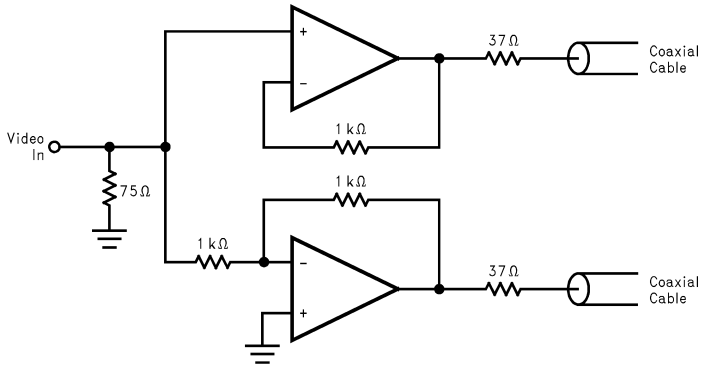
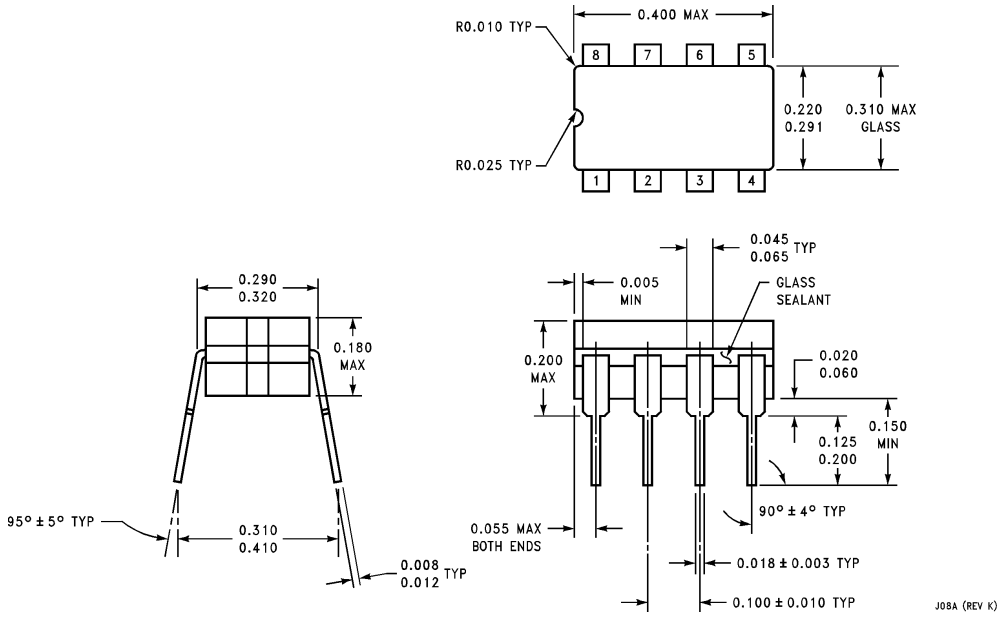
Differential Line Driver

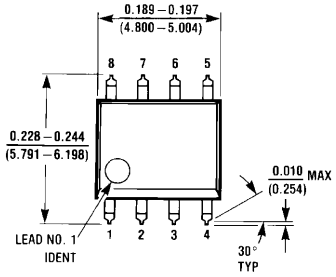


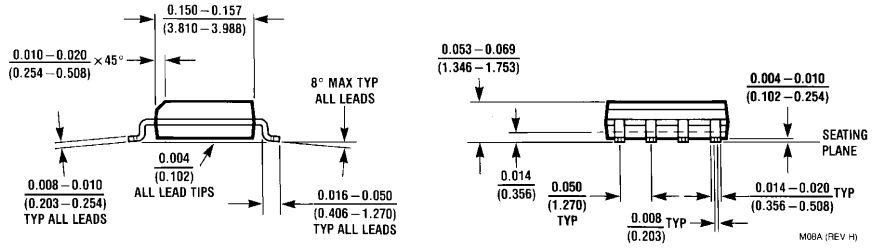
DS012581-49

Physical Dimensions inches (millimeters) unless otherwise noted



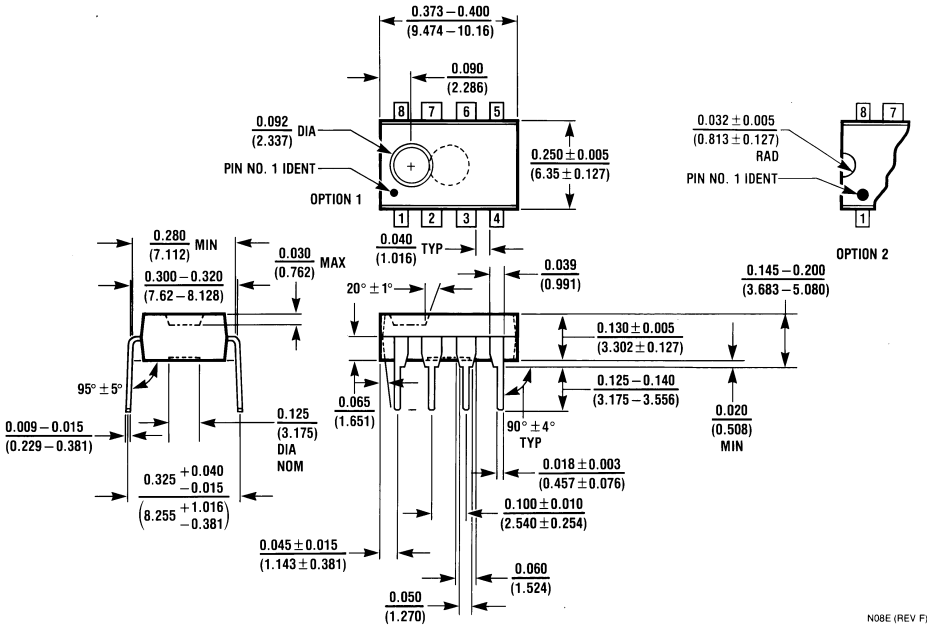
8-Lead Ceramic Dual-In-Line Package
Order Number LM6172AMJ-QML or 5962-9560401QPA
NS Package Number J08A





8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number LM6172IM or LM6172IMX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.300" Wide) Molded Dual-In-Line Package
Order Number LM6172IN
NS Package Number N08E

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