MOTOROLA

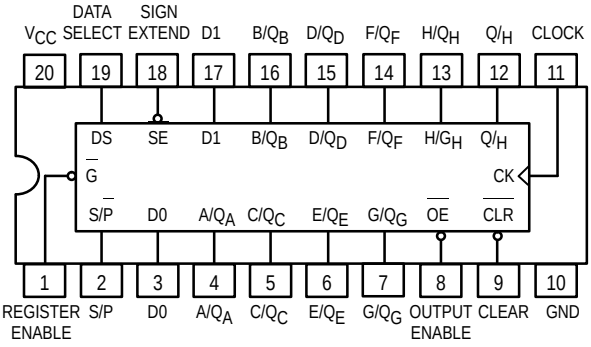
SN54/74LS322A

8-BIT SHIFT REGISTERS WITH SIGN EXTEND

These 8-bit shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D0 or D1 inputs as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/P inputs low. This places the three-state input/output ports in the data input mode. Data is entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_A flip-flop during shifting. An overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

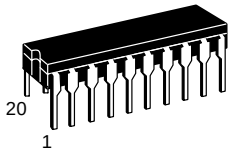
- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Sign Extend Function
- Direct Overriding Clear
- 3-State Outputs Drive Bus Lines Directly

(TOP VIEW)

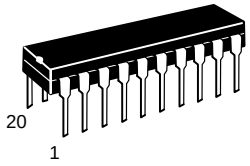


8-BIT SHIFT REGISTERS WITH SIGN EXTEND

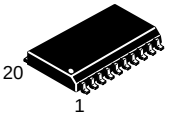
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

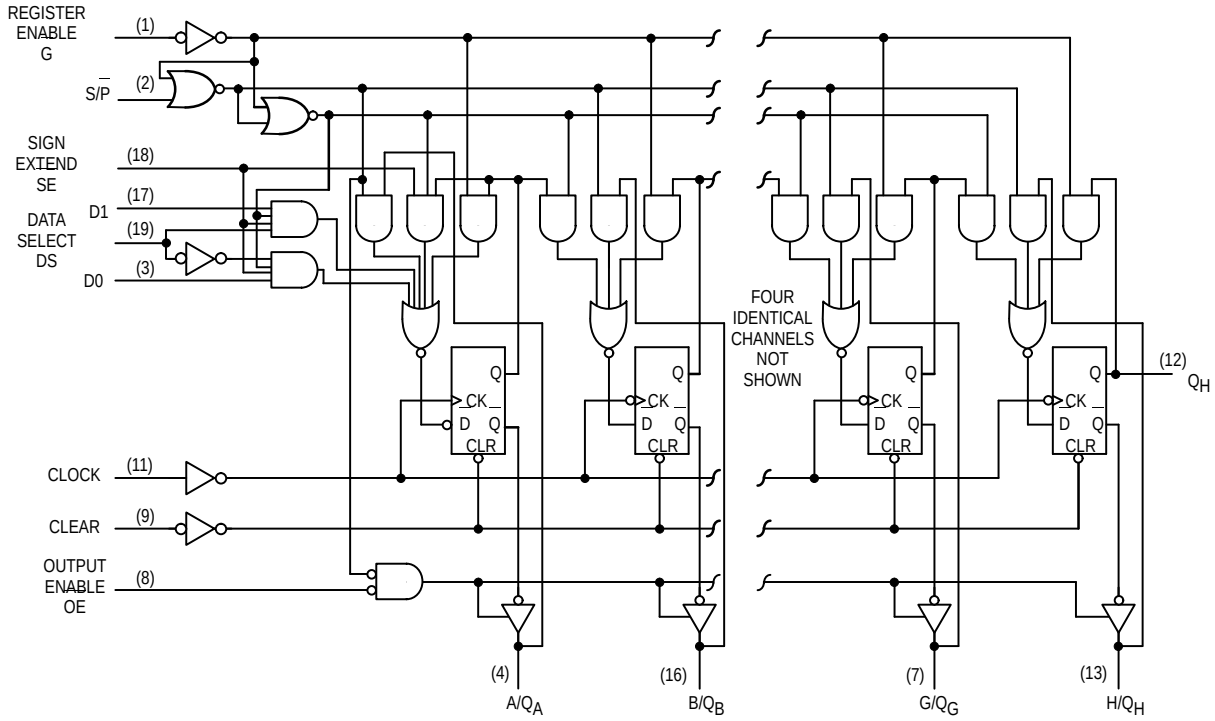
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter			Min	Typ	Max	Unit
V_{CC}	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range		54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	Q_H'	54, 74			–0.4	mA
I_{OL}	Output Current — Low	Q_H' Q_H'	54 74			4.0 8.0	mA
I_{OH}	Output Current — High	Q_A–Q_H Q_A–Q_H	54 74			–1.0 –2.6	mA
I_{OL}	Output Current — Low	Q_A–Q_H Q_A–Q_H	54 74			12 24	mA

BLOCK DIAGRAM



FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT $Q_{H'}$
	CLEAR	REGISTER ENABLE	S/P	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/Q_A	B/Q_B	C/Q_C … H/Q_H		
Clear	L L	H X	X H	X X	X X	L L	X X	L L	L L	L L	L L	L L
Hold	H	H	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}	Q_{H0}
Shift Right	H H	L L	H H	H H	L H	L L	↑ ↑	D_0 D_1	Q_{An} Q_{An}	Q_{Bn} Q_{Bn}	Q_{Gn} Q_{Gn}	Q_{Gn} Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h
When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.												

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW to HIGH level
Q_{A0}…Q_{H0} = the level of Q_A through Q_H, respectively, before the indicated steady-state conditions were established
Q_{An}…Q_{Hn} = the level of Q_A through Q_H, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
a…h = the level of steady-state inputs at inputs A through H respectively

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage Q_A–Q_H	54	2.4	3.2		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.4	3.2		V		
V_{OH}	Output HIGH Voltage Q_H'	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX	
		74	2.7	3.4		V		
V_{OL}	Output LOW Voltage Q_A–Q_H	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
V_{OL}	Output LOW Voltage Q_H'	54, 74			0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74			0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH Q_A–Q_H				40	µA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW Q_A–Q_H				−400	µA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current	Other			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		A–H, Data Select			40	µA		
		Sign Extend			60	µA		
		Other			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		Data Select			0.2	mA		
		Sign Extend			0.3	mA		
		A–H			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current	Other			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Data Select			−0.8	mA		
		Sign Extend			−1.2	mA		
I_{OS}	Short Circuit Current (Note 1)	Q_H'	−20		–100	mA	V_{CC} = MAX	
		Q_A–Q_H	−30		–130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				60	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	35		MHz	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock to Q_H'		26 22	35 33	ns	
t_{PHL}	Propagation Delay, Clear to Q_H'		27	35	ns	
t_{PHL} t_{PLH}	Propagation Delay, Clock to Q_A–Q_H		22 16	33 25	ns	C_L = 45 pF, R_L = 667 Ω
t_{PHL}	Propagation Delay, Clear to Q_A–Q_H		22	35	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 15	35 35	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		15 15	25 25	ns	C_L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width HIGH	25			ns	V_{CC} = 5.0 V
t_W	Clock Pulse Width LOW	15			ns	
t_W	Clear Pulse Width LOW	20			ns	
t_s	Data Setup Time	20			ns	
t_s	Select Setup Time	15			ns	
t_h	Data Hold Time	0			ns	
t_h	Select Hold Time	10			ns	
t_{rec}	Recovery Time	20			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.